

# Tim Weaver

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<http://cudadog.com/tims-portfolio/>

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## Professional Experience:

**Principal Engineer, Co-Owner, Cudadog Designs, Inc., Portland, OR** Aug. 2007 — Present

Responsible for all client engineering services, including Verilog RTL design, simulation, synthesis, verification, debug and technical documentation. Improved client work methods to increase efficiency.

- Designed SPI to AHB bridge
- Built fully automated FPGA tool flows using Synplify Pro and Xilinx
- Provided detailed RTL design and tool flow documentation
- Introduced clients to high level hardware interface methods via Python
- Created cross platform wxPython GUIs to provide easy system register access
- Created remotely hosted FPGA synthesis system
- Synthesized in-house code for speed and size comparison to commercial IP
- Setup multi-board environment used for wireless compliance testing

**Sr. FPGA/ASIC Design Engineer, AudioMojo, Hillsboro, OR** Oct. 2006 — Aug. 2007

Involved in nearly every aspect of home theater wireless audio product development, including architecture and Verilog RTL design, simulation, synthesis, software development, lab debug, customer demonstrations and graphic design. Responsible for the introduction of Mac workstations into engineering. Designed GUIs to accelerate debug and testing.

- Designed I2S interface RTL
- Designed sine wave pattern generator RTL
- Designed white noise generator RTL
- Contributed to audio datapath architecture definition
- Performed all first-level validation for audio datapath
- Created Cocoa GUIs in Python to interface to Altera NIOS processor and register sets

**RTL Design Services (Contract), R2DI LLC, Hillsboro, OR** Jan. 2007 — Feb. 2008

Designed multiple chips used in large-scale multimillion dollar sawmill project.

- Designed SPI slave interface
- Implemented Temposonic linear position sensor interface
- Designed quadrature input and output interfaces

**ASIC Design Engineer, Stexar, Hillsboro, OR** Feb. 2006 — Aug. 2006

Developed SOC components for a custom x86 based video processor.

- Extended AES encryption functionality
- Designed MPEG TSD PVCI/AHB bridge slave interface
- Integrated third party IP
- Performed timing and area analysis using Magma
- Set up FPGA simulation environment

**FPGA/ASIC Design Engineer, Pixelworks, Tualatin, OR** Mar. 2004 — Feb. 2006

Responsible for validation of VHDL based large-scale video processor components on custom FPGA platform. Reduced FPGA bits generation time from one week to four hours.

- Created automated FPGA tool flow to simplify the synthesis procedure
- Generated functional test vectors
- Generated ATPG vectors
- Created PERL scripts for fellow designers to help them solve problems more efficiently
- Created PERL wrapper script for CVS to prevent concurrent editing of certain files

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## **FPGA/ASIC Design Engineer, RadiSys, Hillsboro, OR**

Feb. 1999 — Mar. 2004

Responsible for many aspects of ASIC/FPGA design, testing, synthesis and validation. Responsible for designing custom motherboards for ASIC/FPGA validation. Increased efficiency by automating work flows.

- Designed Verilog RTL for SDRAM analyzer, multi-disk hot-swap/power controller and telecom FPGAs
- Designed Pentium II/III motherboards, and logic analyzer interposer for chipset validation
- Crafted PERL scripts to generate postscript pinout plots used in product specifications
- Optimized FPGA synthesis tool flow using makefiles
- Worked closely with marketing to prepare customer demonstrations and solve customer issues
- Designed a zero maintenance web-based documentation repository using PERL
- Awarded two "All Star Awards" for work excellence and customer service

## **Hardware Design Engineer Intern, RadiSys, Hillsboro, OR**

Jun. 1998 — Aug. 1998

- Assembled and debugged over 40 prototype boards necessary for urgent delivery
- Modified and updated product schematics
- Produced new product data sheet
- Responsible for choosing replacement components

## **Software Designer, CyberHighway Internet Service Provider, Boise, ID**

Jun. 1997 — Aug. 1997

- Created custom Internet applications using PERL and C

Dec. 1998 — Feb. 1999

## **Education:**

### **University of Idaho**

Bachelor of Science in Electrical Engineering. Minor in Computer Science.

Dec. 1998

## **Member:**

### **Portland Area Robotics Society (PARTS)**

Aug. 2001 — Present

- Vice President and Webmaster (Jan. 2004 — Dec. 2005)
- Head organizer of PDXBOT.05
- Member, 2002 – 2005 PDXBOT competition planning committees